

What Is Claimed Is:

1. A liquid crystal display device, comprising:

a liquid crystal display panel for displaying image data corresponding to a digital video signal;

a digital video card for generating the digital video signal, a vertical synchronizing signal and a horizontal synchronizing signal;

a controller for generating a dot clock signal and a dual gate start pulse using the vertical and horizontal synchronizing signals;

a data driver for applying the digital video signal to data lines in response to the dot clock signal; and

a gate driver for applying scanning signals having at least two signal voltage levels to gate lines in response to the dual gate start pulse.

2. The device according to claim 1, wherein the gate driver includes a shift register for sequentially generating scanning pulses in response to the dual gate start pulse, and a level shifter for shifting voltages of a first level of the scanning pulses from the shift register to output voltages of a second level different from the first level.

3. A method of driving a liquid crystal display including a gate driver for sequentially driving gate lines of the liquid crystal display, comprising the steps of:

sequentially generating a scanning pulse in response to a dual gate start pulse;

shifting a voltage level of the scanning pulse to a voltage level for driving the liquid crystal cell;

sequentially applying the shifted voltage level of the scanning pulse to the gate lines; and

charging a pixel of the liquid crystal display with the voltage applied to the gate lines via a storage capacitor.

4. The method according to claim 3, wherein the pixel voltage is a different polarity for each gate line.

5. The method according to claim 3, wherein the shifted voltage level of the scanning pulse is applied to the gate lines during at least two consecutive horizontal period signals.

6. The method according to claim 5, wherein the voltage level of the scanning pulse has at least a two-level difference corresponding to at least a first horizontal period signal.

7. The method according to claim 6, wherein the voltage level of the scanning pulse during a second horizontal period signal is larger than the voltage level of the scanning pulse during the first horizontal period signal.

8. The method according to claim 7, wherein the voltage level of the scanning pulse during the second horizontal period signal is more than twice the voltage level of the scanning pulse during the first horizontal period signal.

9. A method of driving a liquid crystal display, comprising the steps of:

generating a scanning pulse in response to a dual gate start pulse;

shifting a voltage level of the scanning pulse to a voltage level for driving a liquid crystal cell;

applying the shifted voltage level of the scanning pulse to a plurality of gate lines; and

charging a pixel of the liquid crystal display to the applied shifted voltage level via a storage capacitor.



15. A method of driving a liquid crystal display, comprising the steps of:

generating a scanning pulse;

shifting a voltage level of the scanning pulse to drive a liquid crystal cell;

applying the shifted voltage level of the scanning pulse to a plurality of gate lines; and

applying the applied shifted voltage level to a pixel via a storage capacitor,

wherein a voltage level of the scanning pulse during a second horizontal period signal is larger than a voltage level of the scanning pulse during a first horizontal period signal.

16. The method according to claim 15, wherein the voltage level of the scanning pulse during the second horizontal period signal is more than twice the voltage level of the scanning pulse during the first horizontal period signal.

17. A method of driving a liquid crystal display device, comprising the steps of:

generating a digital video signal, a vertical synchronizing signal and a horizontal synchronizing signal;

generating a dot clock signal and a dual gate start pulse using the vertical and horizontal synchronizing signals;

applying the digital video signal to at least a plurality of data lines in response to the dot clock signal; and

applying scanning signals having at least two signal voltage levels to at least a plurality of gate lines in response to the dual gate start pulse.

18. The method according to claim 17, wherein the step of generating a digital video signal, a vertical synchronizing signal and a horizontal synchronizing signal includes a digital video card.

19. The method according to claim 17, wherein the step of applying the digital video signal to at least a plurality of data lines in response to the dot clock signal includes a data driver.

20. The method according to claim 17, wherein the step of applying scanning signals having at least two signal voltage levels to at least a plurality of gate lines in response to the dual gate start pulse includes a gate driver.